for U. S. filing

ABSTRACT OF THE DISCLOSURE

The electronic data processing circuit targets the emulation of a logic function. The circuit comprises a single clock providing time unit signals, a programmable synchronous logic array for processing values on a time unit basis, a means for detecting internal or external value state changes known as events , a means for programming state changes or event signals, a means for processing a series of scheduled times providing the logic array with scheduled time signals depending on the signals from the detection means or the event programming means and the signals from the clock, wherein said processing means can determine subsequent scheduled times having delayed deadlines programmed by the programming means, depending on the signals from said detection means or said programming means. The processing performed by the logic array is thus dependent on the series of scheduled times triggered by internal or external value state changes and by determination of the series of scheduled times.